Experiment #4

Group 3

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**Abstract**— working with Verilog, Audio processing, working with FPGAs, DAC, ADC, Echo Synthesizing Principles, Playing a Sound, FIFO Structure

Keywords— DAC, ADC, FIFO, FPGA, Sound, Echo.

1. Introduction

In this experiment, we got familiar with the audio processing concepts using FPGAs. In order to do this we first learned about DAC and ADC converters in order to be able to process a signal, which was not digital inside the FPGA, and to see a digital signal outside the FPGA.

We then moved on to echoing sound signals using delays, which we were to be provided using a FIFO.

II. Methodology and Procedures

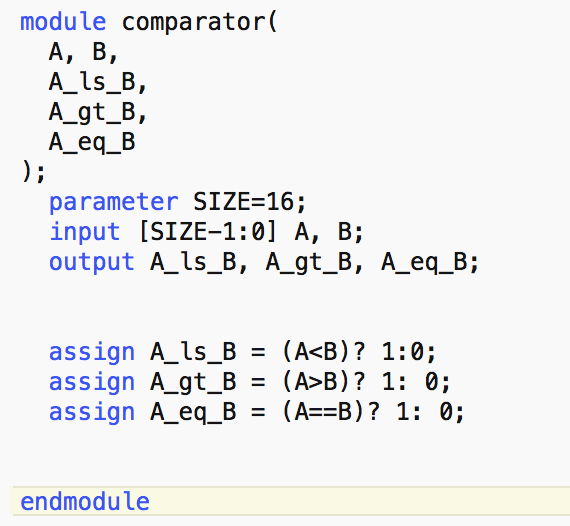
Procedures we took to make this experiment work were as follows:

We first coded a comparator, we tried to pay attention to the fact that the number of bits the numbers which were meant to be compared had would change in time because in order to test it we were going to use 8 bit inputs but then it was to be used as an one bit comparator so we in order to support this functionality we made the unit parameterized.

III. Results

A. Part One

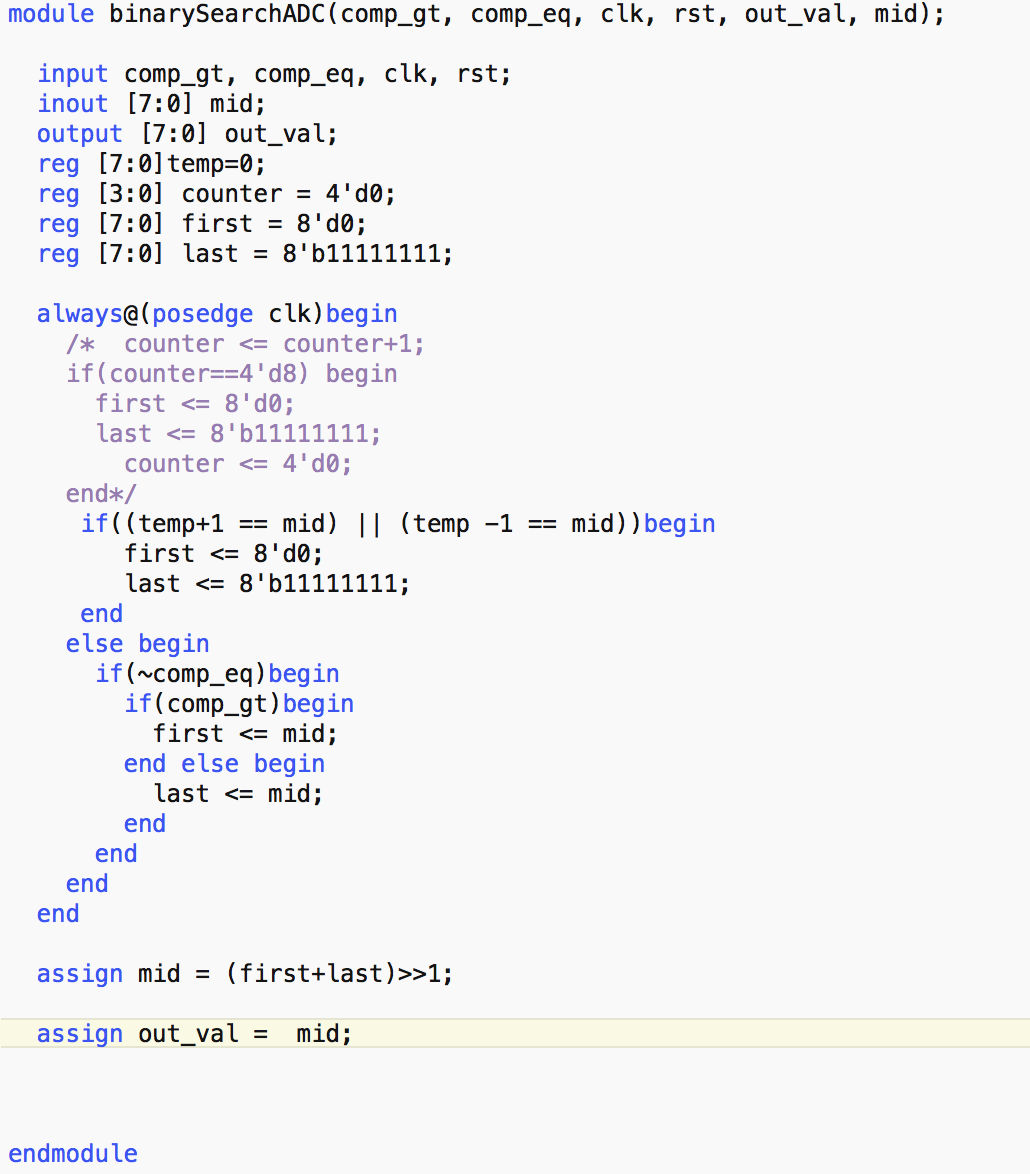
In this part we learned about different implementation methods of an ADC converter. The method we were to implement was the one using a binary search unit. We first designed a comparator shown in figure 1.



**Figure 1: comparing unit**

This comparing unit returns three less than, greater than and equal signals indicating the state of greatness between the two inputs, it is also parameterised so it can be used for any two inputs with any number of bits as long as they have equal number of bits.

We then coded the binary search unit.



**Figure 2 : comparing unit**

B. Part Two

As

C. Waveform Generator

D. Total Design

After

IV. Conclusion

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